WHAT IS CLAIMED IS: -

1. A semiconductor device comprising:

a memory for storing data; and

a logic circuit for controlling the data,

wherein the memory and the logic circuit are constituted by TFTs, and are integrally disposed on a same insulating substrate.

2. A device according to claim 1, wherein the memory is a nonvolatile memory.

3. A device according to claim 2, wherein the nonvolatile memory includes a plurality of FAMOS type TFTs.

4. A device according to claim 1, wherein an active layer of each of the TFTs has a thickness of 10 to 100 nm.

5. A semiconductor device comprising:

a memory for storing data; and

a logic circuit for controlling the data,

wherein the memory and the logic circuit are constituted by TFTs, and are integrally disposed on a same insulating substrate; and

wherein an active layer of each of the TFTs has a

thickness of 10 to 100 nm so that it becomes easy to carry out impact ionization.

6. A device according to claim 5, wherein the memory is a nonvolatile memory.

7. A device according to claim 6, wherein the nonvolatile memory includes a plurality of FAMOS type TFTs.

8. A semiconductor device comprising:

a control circuit for carrying out gamma correction of a supplied signal; and

a memory for storing data used in the gamma correction,

wherein the control circuit and the memory are constituted by TFTs, and are integrally disposed on a same insulating substrate.

9. A device according to claim 8, wherein the memory is a nonvolatile memory.

10. A device according to claim 9, wherein the nonvolatile memory includes a plurality of FAMOS type TFTs.

11. A device according to claim 10, wherein the signal is a digital signal.

12. A device according to claim 10, wherein the signal is an analog signal, and the semiconductor device further comprises a conversion circuit for converting the analog signal to a digital signal.

13. A semiconductor display device comprising:

a pixel region in which a plurality of TFTs are arranged in matrix;

a driver for switching the plurality of TFTs;

a picture signal supply source for supplying a picture signal;

a control circuit for carrying out gamma correction of the picture signal; and

a memory for storing data used in the gamma correction of the picture signal,

wherein the plurality of TFTs, the driver, the control circuit, and the memory are integrally disposed on a same insulating substrate.

14. A device according to claim 13, wherein the memory is a nonvolatile memory.

15. A device according to claim 14, wherein the nonvolatile memory includes a plurality of FAMOS type TFTs.

16. A device according to claim 15, wherein the picture signal is a digital signal.

17. A device according to claim 15, wherein the picture signal is an analog signal, and the semiconductor display device further comprises a conversion circuit for converting the analog signal to a digital signal.

18. A device according to claim 16, wherein an active layer of each of the TFTs has a thickness of 10 to 100 nm.

19. A semiconductor display device comprising:

a pixel region in which a plurality of TFTs are arranged in matrix;

a driver for switching the plurality of TFTs;

a digital picture signal supply source for supplying a digital picture signal;

a conversion circuit for converting the digital picture signal to an analog signal;

a control circuit for carrying out gamma correction of the digital picture signal; and

a memory for storing data used in the gamma correction of the digital picture signal,

wherein the conversion circuit includes a plurality of

voltage lines for supplying different voltages to source lines of the plurality of TFTs; and

wherein the plurality of TFTs, the driver, the control circuit, and the memory are integrally disposed on a same insulating substrate.

20. A device according to claim 19, wherein the memory is a nonvolatile memory.

21. A device according to claim 20, wherein the nonvolatile memory includes a plurality of FAMOS type TFTs.

22. A device according to claim 21, wherein an active layer of each of the plurality of TFTs has a thickness of 10 to 100 nm.